Fairly Quick VMEbus Digitizer

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Introduction

This is a short description of a proposed general purpose VMEbus multi-channel digitizer board optimized to acquire data for accelerator studies. Consideration of this design is the result of discussions with Vinod Bharadwaj and Elliot McCrory.

Current "fast" digitizer capabilities available in Fermilab control systems are limited to either a few kHz for normal data acquisition or readout of a single or dual channel commercial digital storage oscilloscope. Between these two limits, there is a need for devices that can digitize several channels at rates up to a few tens of megahertz and store several thousand readings for each channel.

Typical Applications

Two typical example application areas are: 1) reading Booster data once per revolution throughout the entire cycle, and 2) reading the waveform of several Linac parameters during individual Linac cycles. For the Booster case, the digitizer must convert in 3.5 μs to 1.6 μs (injection to extraction revolution period) and store about 25,000 readings for a complete Booster cycle. If a residual gas profile monitor was to be read, 32 channels would be needed. For the Linac case, to digitize a hundred samples during a 50 μs Linac beam pulse, a 2 MHz rate is needed. Because only part of the memory is used each cycle, the digitizer could be gated "on" for 100 μs each Linac pulse, and data collected from 16 successive pulses could be stored in a few kBytes memory. This mode is useful to study whether beam properties of the Linac are the same on all 13 Linac cycles of a given Main Ring injection sequence.

The design of such a digitizer system is a compromise of cost versus resolution, digitize rate, memory depth, and number of channels per board. Although, very fast sample rates are possible, the cost of both the digitizers and the associated memory rise rapidly as the speed is increased. If 8-bit resolution is adequate, the 20 MHz digitizer and the associated 50 ns memory are modestly priced. Twelve bit digitizers are more expensive, double the amount memory needed, and reduce the number of channels per board, but many applications require the 12 bit resolution. This paper describes a 12-bit 2 Mhz version.

Board Design

The present design, shown in Figure 1, includes four digitizer-memory channels, the programmable trigger and digitizer clock logic, and the VMEbus interface. This design uses the 12-bit 1-MHz Datel model ADS-112 digitizer with 128 k Bytes (64k samples) of memory for each of the four channels. The vendor expects the performance of this digitizer to be increased to 2-MHz within a few months. The resulting board appears to the bus as a 512K byte RAM card and a few registers in VMEbus I/O space for trigger, digitizer clock and gate control. Memory and registers may be accessed from VMEbus as either bytes or words. Provision is made for using internal or external triggers, digitizer clocks and gate signals.

Three 16-bit R/W parameter registers, located in VME I/O space, are as follows:

Control and Status Register: This bit-significant register selects the operating characteristics of the board.

Location Counter: A pointer to the next data sample location to be filled with the digitizer data.

Gate Duration Counter: The number of conversions to be performed following a Trigger event.

The contents of the bit-significant Control-Status register selects the operating characteristics of the board as defined below:

Bit 15: 1= Digitizer active
Bit 14: 1=Digitizer armed to run (or stop) when triggered
Bit 13: 1=Circular Buffer mode enabled
Bit 12: 1=Wrap mode enabled

Bit 11: 1=Auto-Reset Location Count
Bit 10: 1=External Trigger enabled
Bit 9: 1=External Gate enabled
Bit 8: 1=External Digitize clock enabled

Bit 7: Software Trigger (Writing a '1' causes a Trigger)
Bit 6-4: Unassigned
Bit 3-0: Digitize Rate Selector

Operation

Note that this is a "dumb" board that does not require programming a microprocessor to operate. Using the simple architecture described here, several operating modes are possible, each of them defined by setting values into the above registers :

Normal Mode: In the Normal mode, digitizing begins at the external or the selected rate following a trigger and fills the number of memory locations given by the *Gate Duration Register.* The *Auto-Reset* bit of the C/S register determines whether the location counter is reset by a trigger event. When the *Location Counter* is not reset each trigger, data following successive triggers is stored sequentially in memory until the memory is filled. If *Auto Reset* is on, old data is overwritten by new data each time a trigger is received.
The *Wrap* bit in the C/S register determines if the digitizer stops at the end of memory or wraps around and begins to fill memory at location zero. If the *Wrap* bit is off and the memory has been filled, additional triggers are ignored so the host computer can process the captured data at its leisure.

Circular Buffer Mode: In this mode, the digitizer continuously fills memory and is stopped by triggering. As in the Normal Mode, the number of conversions that follow the trigger is given by the value stored in the *Gate Duration Register*. This allows the capture of data both before and after a trigger, and the trigger may be located at any point within the captured data set.

Convert Strobes: It is assumed that all four channels will be digitized at each clock event. There is a separate pin on the control chip for the clock input for each channel so that the external clock pulse can be run through a multi-tap delay line to accommodate skew in the input signals.

VMEbus Addressing: The digitizer board occupies 512k Bytes of memory space, and 256 bytes of short I/O space. The memory and I/O addresses are selected by a thirteen-section and an eight-section DIP switch, respectively.

Miscellaneous: Analog inputs may be brought onto the board through either the front panel or the rear P2 connector. Jumpers are provided to select 50 ohm termination for each of the input signals. The analog input range is jumper selectable 0-10V or ±5V.

The internal digitize clock is derived from the VMEbus 16 MHz bus clock or from an optional onboard oscillator. After a divide by four, either this clock or the external clock may be selected as input to a 16-bit counter. Any one of the sixteen binary related frequencies can be selected as the digitize rate by setting the bit number into bits 0..3 of the Control register, so that digitize frequencies of 4 MHz, 2 MHz, 1 MHz, 0.5 MHz,... are available.

In the context of the VMEbus-based Linac control system, the digitizer board does not impact the software of the local stations. Digitizer boards could be installed in any of the systems and operated by application

programs written for either the Sun computer or the VAX console. The local station simply provides the path to access digitizer memory over the Token Ring network. A Memory Data list type is used to request information from any digitizer .

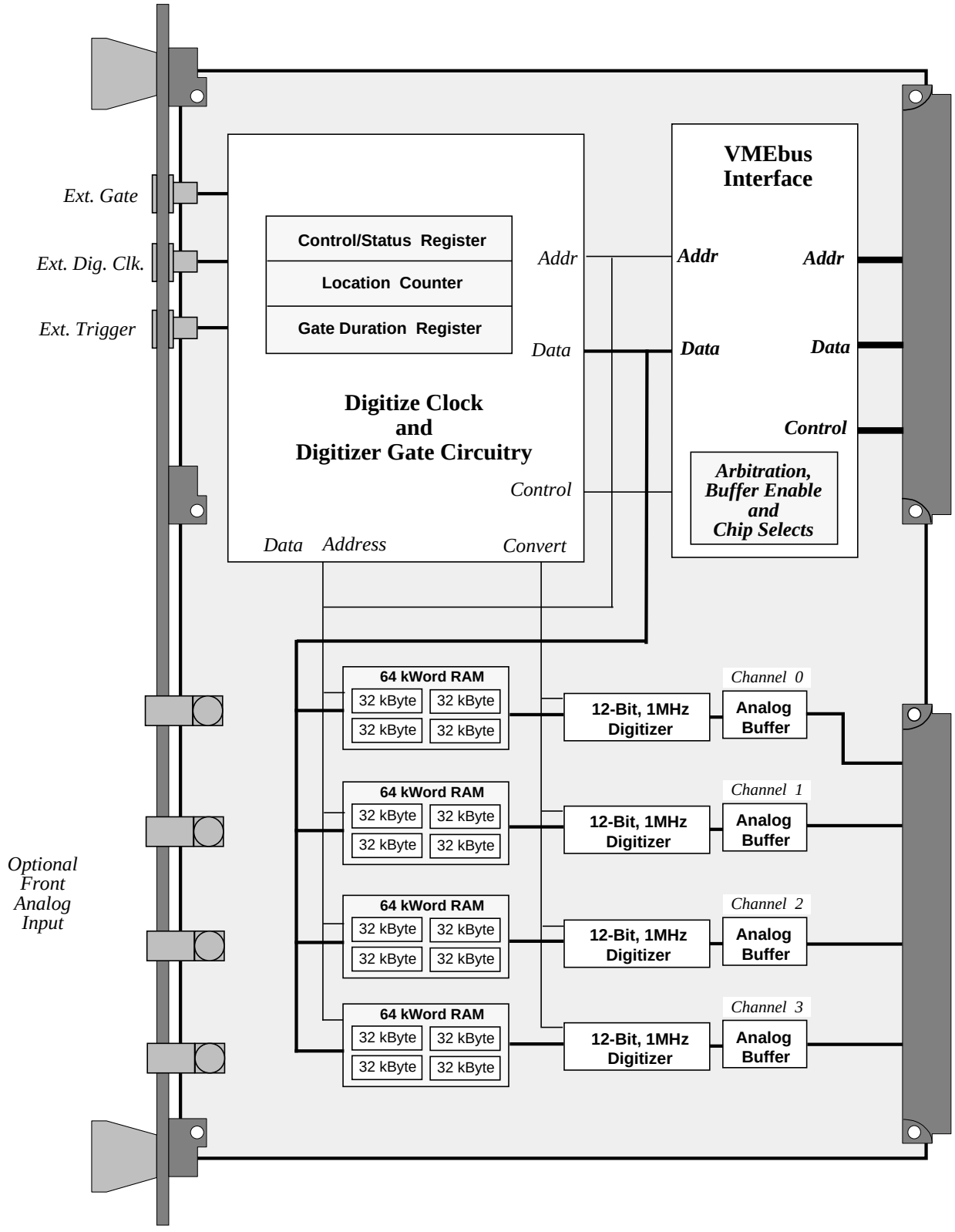
Implementation Details

The board described here has been designed. The control circuitry is contained in an Actel 1020A programmable gate array, a user configurable 2000 gate array chip. Using this chip, the functionality of the board is all contained in a single part and can be modified without changing the the pc board layout.

VMEbus Addressing: Memory on the board is accessed as four blocks of contiguous Read/Write RAM for a total of 512k Bytes per board. Both byte and word accesses are supported. Base address of the memory is set by a 13-bit DIP switch.

The *Control/Status Register*, the *Sample Counter*, and the *Gate Duration Register* occupy three consecutive words of memory located in VMEbus I/O space at *Base+0*, *Base+2*, and *Base+4*, respectively. An 8-bit DIP switch sets the upper eight bits of the 16-bit I/O base address. These registers may only be accessed as bytes of memory. Word access to these registers is not supported.

A/D Convert Pulses: Internal operation of the control gate array requires that all four A/D channels be triggered once for each clock pulse. If the external delay feature is implemented, time skewed signal may be aligned by jumpering the convert pulse inputs to various outputs of a tapped delay line. If no delays are needed, the four channels can all be triggered at *External Clock* time. For triggering using the internal time base, the four channels will trigger simultaneously. Requiring all four channels to convert each time allows the control chip to store data in memory after the conversions are finished, in order to keep digital noise from one channel from affecting the conversion of other channels.



VMEbus 4-Channel Fairly Quick Digitizer

1 MHz Conversion Rate

mf. 053090